# Fabrication of low-loss SOI nano-waveguides including BEOL processes for nonlinear applications

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We report successful fabrication of low-loss SOI nano-waveguides with integrated PIN diode structures. The entire fabrication process is done on a 200 mm BiCMOS toolset using front-end-of-line (FEOL) and back-end-of-line (BEOL) processes and does not show any undesirable influence upon the photonic performance. Such a waveguide technology forms an attractive platform for a wide range of nonlinear applications due to efficient free carrier removal as well as use of standard substrates and processing technology. Nonlinear experiments were conducted to investigate the potential of the introduced technology. The performance of the designed waveguides can be used as a benchmark for future development of proposed platform for integrated silicon photonics and electronics circuits.
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**Keywords:** photonic integrated circuits, waveguide, nonlinear optics

## 1 INTRODUCTION

Recognized as a promising innovative field, silicon photonics has gained a lot of interest during the last decade. One of the key merits of this technology is that photonic integrated circuits (PIC) can be fabricated using the existing complementary metal-oxide-semiconductor (CMOS) technology base. In recent years, a lot of activity has been dedicated to all-optical or nonlinear studies deploying silicon waveguides. Many applications have been explored, mainly for telecommunication and optical interconnects such as all-optical switch, modulators, and Raman lasers [1]–[7]. However, nonlinear optical applications of the silicon material system have been severely hampered by effects associated with free carriers that are inevitable created due to two-photon absorption (TPA). Free carriers pose a serious challenge to nonlinear devices using continues wave (CW) light in the telecom wavelength range, which is of course highly relevant to the communications sector. Recently, we demonstrated by means of 3D device simulations that free carrier lifetime can be reduced by several orders of magnitude in silicon nano-waveguides with dedicated PIN structures [8, 9]. Nano-waveguides are the most prominent candidates for nonlinear applications because here the highest optical intensities can be achieved of the whole spectrum of silicon waveguides ranging from SOI of 10 µm thickness down to nano-waveguides. We could also show numerically that the nonlinear figure of merit could be increased by one order of magnitude if the PIN structure was combined with shallow-etched nano-waveguides that show very low linear loss, as was recently demonstrated by W.Bogaerts et al. and P. Dong et al. [10, 11]. The present paper will provide a first overview of the nano-waveguide technology platform that we developed to meet the pre-requisites of a high-performance nonlinear silicon photonics technology, i.e. nano-waveguides with low linear loss combined with PIN diodes. The development followed the numerically established design rules [8]. The advantage of this approach compared to other techniques that increase nonlinear efficiency is the use of standard SOI-material, which is fully compatible with additional thermal budgets typically encountered at later stages of device fabrication or integration.

In this paper, we shall first present nano-wire strip waveguide fabrication and comparison with state-of-the-art. Then we will demonstrate both shallow and deep-etched nano-waveguides with rib geometry fabricated with embedded PIN structures and analyze the integrated waveguide performance. At last, we shall show a promising application in nonlinear silicon photonics for such photonic and electronic integrated waveguide circuits. All the nano-waveguides are fabricated using IHP's BiCMOS technology toolset in a 200 mm-wafer pilot production line using deep UV lithography (248 nm).

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## 2 NANO-STRIP WAVEGUIDE FABRICATION AND COMPARISON WITH STATE-OF-THE-ART

Typical SOI nano-strip waveguide can be shrunk down to sub-micrometer cross-section but still maintain strong confinement of light, which enables designs with very small waveguide bends. At telecommunication wavelengths around 1550 nm, experimental results have shown that strip waveguides with a height of around 220 nm and width of around half micrometer exhibit negligible bending loss for bends with radius down to only a few microns [12]. These nano-wires have greatly improved waveguide integration density. However, such nano-waveguides also have disadvantages. One of the key figures of merit in PICs is linear waveguide loss, which depends mainly on the interaction between the optical mode and the sidewall surface roughness. The large refractive index contrast significantly increases this scattering loss [13]. With electron-beam fabrication, it is possible to reach a linear loss around 1 dB/cm, which is, however, not compatible with the technology of electronic IC production [14]. Most experimental results show that in general it is difficult to reach losses lower than 2 dB/cm using stepper fabrication based on deep UV lithography.

Nano-strip waveguides were fabricated on SOITEC 200 mm SOI wafers with a 2000 nm buried oxide (BOX) layer and 220 nm slightly P-doped crystalline silicon layer on top. Two layers of silicon nitride and thermal oxide were deposited as the hardmask for the subsequent etching of waveguides. The wafer was then coated with photo-resist and exposed by 248 nm Deep-UV scanner. After development and etching, the pattern was transferred to the hardmask and the waveguide was etched through the hardmask down to the BOX layer. The thickness of the hardmask and the recipes of each etching step have been optimized to minimize the sidewall surface roughness. The entire process is completely compatible with IHP 0.25 μm BiCMOS technology. Cut-back measurements were performed at a wavelength of 1550 nm with waveguides of different lengths on the same chip to extract loss values. To this end we designed a set of nano-strip waveguides with a core dimension of 450 nm(w) x 220 nm(h) and with length varying from 0.5 cm to 6 cm. This geometry supports a single quasi-TE mode. As shown in Figure 1, each point represents one cut-back measurement with a waveguide of a certain length. The slope of the linear fit indicates the linear propagation loss is 1.7 dB/cm. Additional measurements from different wafers and designs show typical loss values for the present SOI nano-wire technology below 2 dB/cm, which corresponds well with the state-of-the-art. The intercept of the vertical axis in Figure 1 reveals the coupling loss. In the cut-back measurement, light was coupled in and out of the waveguide through a standard single-mode-fiber (SMF) via a grating coupler and a following taper to the nano-waveguide. Power at coupling-in was about 3 dBm, as determined from back-to-back measurements. The grating coupler was designed for TE polarization and fabricated prior to the waveguides using an additional lithographic step. It consists of 25 periods with both ridge width and groove width of 315 nm and etching depth of 70 nm, which is optimized for wavelength of 1550 nm. The statistics of measurement results

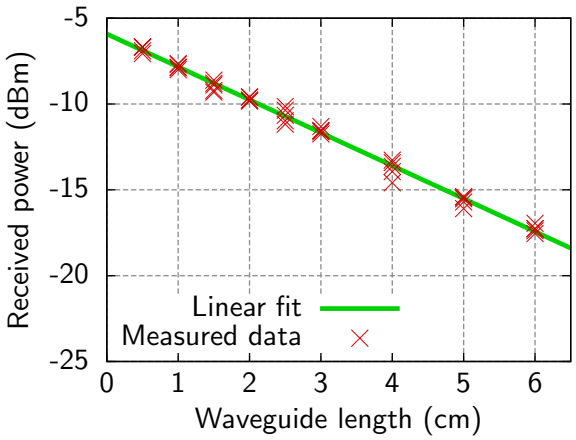


FIG. 1 Cut-back measurement results for 450 nm waveguides. Each symbol represents a TE-transmission signal through a waveguide with a certain length. The solid line is the linear fit showing a loss of 1.7 dB/cm.

from a set of wafers show that the insertion loss is 4.4±0.7 dB, which is typical for grating couplers. The etch depth variation is within ten percent.

Dispersion is of distinct importance for many applications. In Figure 2(a) we present the numerically determined effective index for each guided mode ($\lambda$=1550 nm) in the SOI waveguide with fixed height of 220 nm and varying width between 0 to 3 micrometers. The simulation was done using JCMsuite [23]. The color of different dot represents the hybridness of the mode, which is defined as the ratio between Ex and Ey (electric field component in x and y direction, respectively). In the design, we chose the geometry of the waveguide to only support one fundamental mode. With increasing waveguide width more modes will appear and these additional modes will become quasi TE/TM ultimately when the waveguide gets wider. As it is seen in the graph, the effective index is very sensitive to the variation of waveguide geometry. In particular, for the narrow nano-wires below 500 nm width, the effective index of the quasi-TE mode changes extremely rapidly with only a small variation of the waveguide width. On account of the strong sensitivity of effective index to the waveguide geometry, it is necessary to achieve a tight control of the tolerance of the waveguide geometry if optical designers intend to obtain a desired propagation property of light wave. The most important waveguide parameter here is the group index. Figure 2(b) depicts the simulated dependence of the group index on the waveguide geometry for the fundamental quasi-TE mode when dimensions width and height differ from the standard 450 nm x 220 nm. Therefore, the target geometry is in the center of the figure, indicating a group index of 4.39 for the designed waveguide. The ranges in the figure are ±50 nm for width and ±20 nm for height. The contour lines correspond to waveguide geometries of constant group index. Figure 2(b) shows that the variation of group index for the first quasi-TE mode is mainly influenced by the width change of the waveguide rather than height variation. If we take into account a fabrication error tolerance of ±10 nm around the target wire width (450 nm), the variation of group index is around 0.04, i.e. 0.9%. Another factor which affects the group index is the transmission wavelength. A measure-

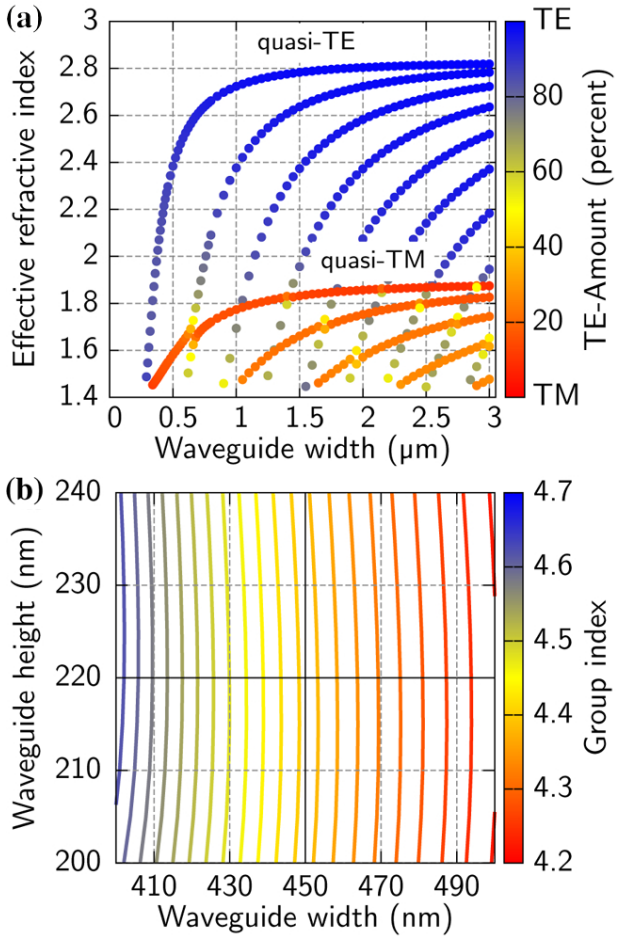


FIG. 2 (a) Numerical effective indices for the first guided modes in nano-strip waveguides as a function of waveguide width. The color indicates hybridness of the mode. (b) Numerical group index versus the waveguide geometry for the fundamental quasi-TE mode around the standard dimensions (450 nm x 220 nm). The contour lines represent waveguide geometries of constant group index.

ment of group index (quasi-TE mode) for the C-band is shown in Figure 3. The group index was experimentally determined as follows: We measured the filter curve (i.e. transmission vs wavelength) of a delay interferometer structure with fixed geometric delay. From the filter curve we determined the wavelength dependent free-spectral range (FSR). The FSR is inverse proportional to the group index following the relation $FSR = \frac{\lambda^2}{L \cdot n_g}$. These measured data correspond to a dispersion

$$\frac{d\tau}{d\lambda} = \frac{1}{c_0}\frac{dn_g}{d\lambda} \approx 5\frac{ps}{nm \cdot m} \quad .$$

A variation of waveguide geometry would result in an offset of the measured characteristics, which is verified by the simulation results (dashed lines). There is a slight increase of group index for larger wavelength and the variation of group index through the whole C-band is about 0.07. Measurement of the group index within a certain wavelength range permits to determine the waveguide fabrication error.

## 3 FABRICATION OF E/O WAVEGUIDE PLATFORM

So far, we considered a plain waveguide technology with process steps realizing just waveguides and coupling structures.

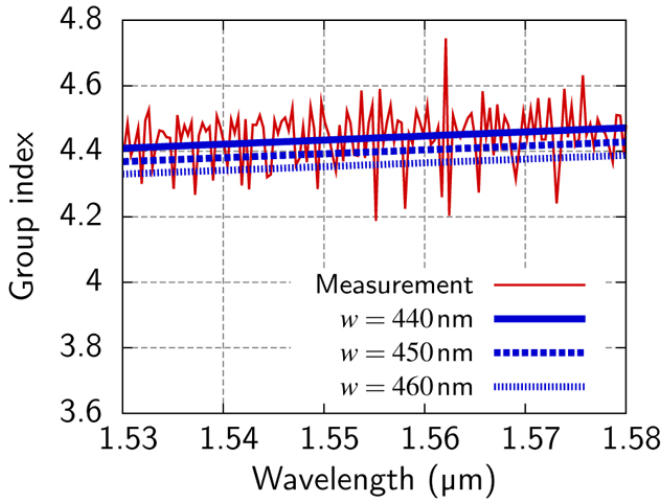


FIG. 3 Measurement and simulation results of group index dependence on wavelength in C-band for standard waveguide. The dashed lines represent numerical results for waveguides of varying width (440 nm, 450 nm and 460 nm).

If we want to introduce electro-optic functionality such as waveguide-diode structures, additional process steps are required. The first important step is to design the waveguide diode fabrication process. This is followed by integration of the photonic process with an electronic back-end process. Our electronic baseline process is a 0.25 μm CMOS technology. Therefore, the task is to integrate the 0.25 μm CMOS contact module together with the waveguide diode structures. In order to avoid problems such as damage of the photonic devices or contact issues between photonic devices and the metal electrodes, careful process integration is mandatory. This leads to a process cross-section as depicted in Figure 4.

The E/O waveguide was designed as a rib-waveguide with PIN junction embedded. Waveguide length varied from 1cm to 4 cm. Figure 4(a) illustrates the schematic geometry of the device. The integrated structure was fabricated on 220 nm SOI substrates. The first step was etching the grating coupler, using a SiNO layer as a hardmask. The etching depth of the grating was 70 nm. Then the waveguides were etched with a width of 500 nm using the same hardmask as for previously presented nano-wires. However, instead of etching down to the BOX, a 50 nm slab (deep etched) or 150 nm slab (shallow etched) of silicon was kept. For both lithography steps wafers were exposed by the 248 nm Deep-UV scanner. After the waveguide fabrication, two implantation steps with medium level doping concentrations ($\sim 10^{18}/\mathrm{cm}^3$, 600 nm to the middle of waveguide) in the slab were performed to form the diode as shown in the figure. Two additional implantation steps with high doping concentrations ($\sim 10^{20}/\mathrm{cm}^3$) to define the contact area, completed the diode formation. Then, following salicidation W-contact plugs were realized on top of high-dose implanted areas to allow for connection to metal pads. Finally, metal layer corresponding to standard Metal 1 (Al) was deposited and the whole wafer was passivated with SiN. Figure 4(b) shows a focused ion beam (FIB) image of the cross section of the designed structure. The metal electrodes are connected to the $p^+$-doped and $n^+$-doped regions via the contact plugs that have the shape of inverted cones.

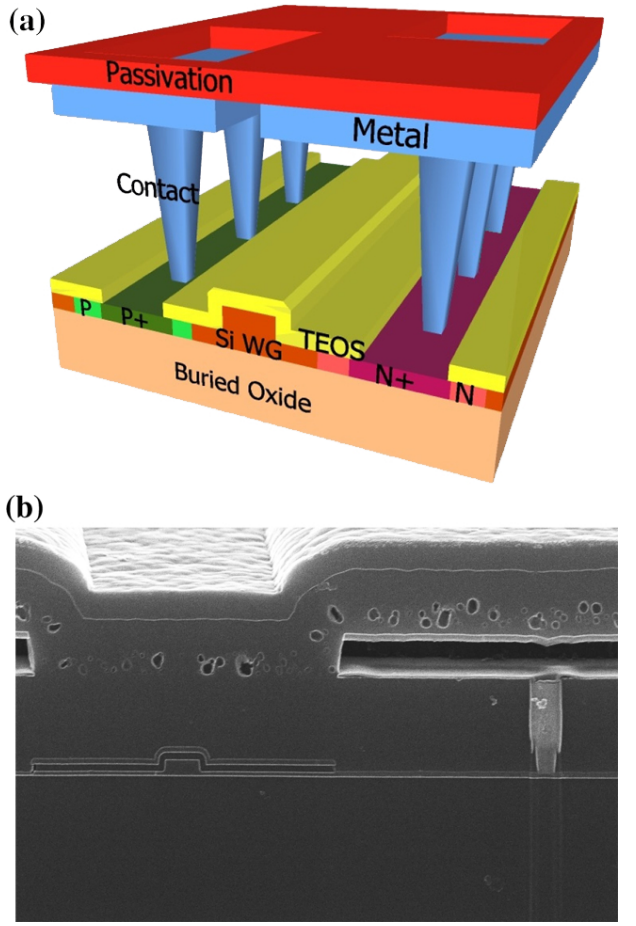


FIG. 4 (a) Schematic geometry of the E/O waveguide. (b) FIB image of the cross section.

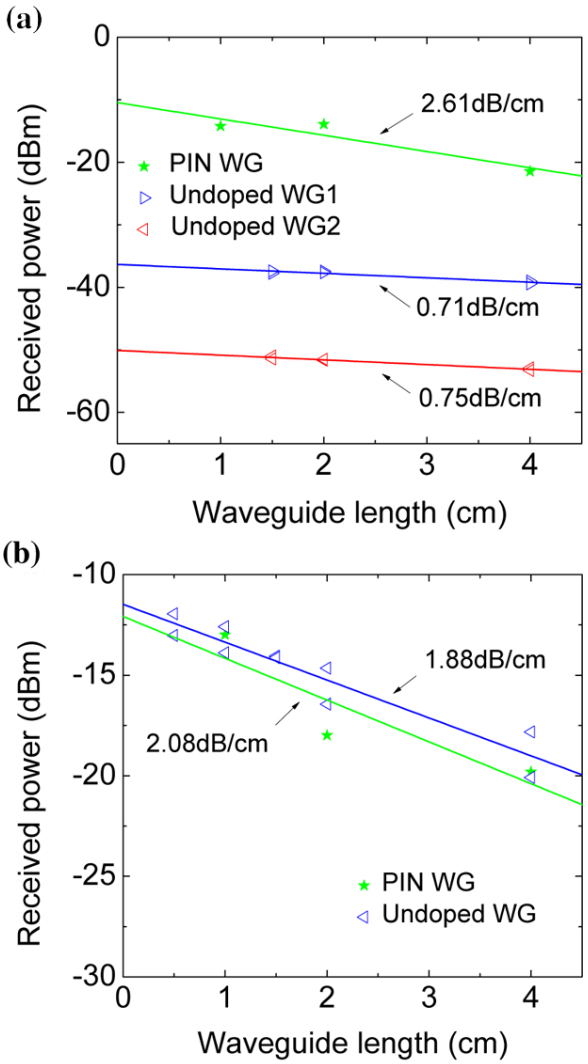


FIG. 5 Cut-back measurement results for (a) shallow etched waveguides and (b) deep etched waveguides. The green symbols represent TE-transmission signals for waveguides with embedded PIN and the slopes of the fitting lines show the losses for (a) shallow etched waveguides and (b) deep etched waveguides, 2.61 dB/cm and 2.08 dB/cm, respectively. The blue and red symbols represent the measurement results for undoped waveguides. The losses are indicated in the figures.

## 4 MEASUREMENT AND ANALYSIS OF INTEGRATED WAVEGUIDE PERFORMANCE

The loss of the proposed designed E/O waveguides was measured again by cut-back measurements. In order to analyze the collateral effect of doping on the light propagation loss, undoped waveguides were also designed without metal contact as a reference. Figures 5(a) and 5(b) present the experimental results for both designed waveguides with shallow etching depth (70 nm) and deep etching depth (170 nm), respectively. The slope of the linear fitting curve indicates the linear propagation loss for the guided mode in waveguide. Various studies showed that shallow etched waveguides have a lower propagation loss parameter compared to silicon wires [11, 15]. The linear propagation loss is mainly due to interaction between the modal field and the sidewall roughness of the waveguide. Shallow etched waveguides have less sidewall surface and the optical modal profile is much more extending to the slab, whereas the mode profile of deep etched waveguides resembles more closely that of strip waveguides with similar core cross section. As it is shown in the figures, the linear loss of shallow etched undoped waveguide is more than 1 dB/cm smaller than that of deep etched undoped waveguides, which agrees well with previously reported experimental results [10]. The linear propagation loss of our samples is still slightly higher than record values of around 0.33 dB/cm. We attribute this to the dependence of propagation loss on the waveguide cross section. Lowest loss values were reported for a rib waveguide with width of 700 nm and etching depth of 70 nm. The rib waveguides we present here had a width of 500 nm, which means that the optical mode field is more highly confined in the rib region and therefore there is more sidewall scattering increasing the linear loss [10]. One disadvantage of the shallow etched waveguides is that they lose the benefit of extreme sharp bends, resulting from reduced modal confinement, which will reduce the photonic circuit compactness. One possible solution for that could be to use hybrid design, as proposed by W. Bogaerts et al, which is a combination of rib straight waveguide and strip nano-wire bend [10]. Regarding linear loss and compactness we therefore conclude that further optimization of the here presented E/O waveguide technology for nonlinear applications is feasible. The insertion loss (defined by the vertical intercept) of the studied sets of undoped waveguides differed due to varying dimensions of the deployed grating couplers. The loss measurement was performed with light of 1550 nm wavelength; however the grating couplers were designed for other wave-

lengths due to the desired application of the designed structure.

Doping of silicon can dramatically increase the optical loss due to the free carrier absorption (FCA), as it was discussed by R. Soref, based on the Kramers-Kronig relation and experimental result [16]. As derived from this model, doping concentration of about $10^{17}/cm^3$ will increase the absorption coefficient to about 3 dB/cm. In rib waveguides doping in the slab might result in additional waveguide loss. The characteristics plotted in Figure 5(a) show that there is an additional loss of about 1.9 dB/cm for shallow etched waveguides with PIN junction embedded. Although the rib itself was not doped, there is an overlap between the optical mode profile and the doped slab region. In comparison, as depicted in Figure 5(b), deep etched waveguides do not exhibit a significant additional loss caused by doping in the slab. This is due to an increased confinement of the optical mode in the waveguide leading to a strong decrease of overlap with the doped slab region.

All the cut-back experiments we discussed above were performed without applying electric bias. One may notice the loss of deep etched E/O waveguides is very close to that of single nano-wires without BEOL process (see Section 2), i.e the BEOL process does not cause significant additional loss. As it is seen in Figure 4(b), the BEOL process implements one additional thick metal layer (about 500 μm) as well as many contact plugs. The cut-back measurements therefore confirm that the BEOL process for the designed E/O waveguides was implemented appropriately.

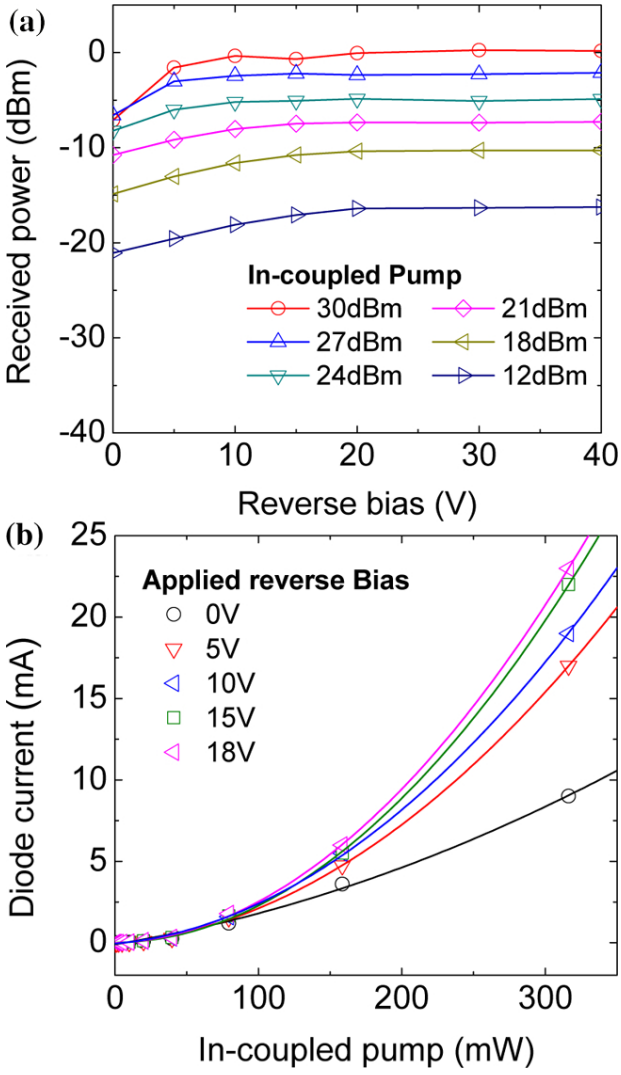


FIG. 6 Experimental results from the deep-etched E/O waveguide of 4 cm length. (a) Received power versus applied reverse bias voltage for different in-coupled pump power. Power values were measured by optical spectrum analyzer and therefore attenuated by 14 dB. (b) Diode current as a function of the in-coupled pump in the waveguide for different applied reverse bias. Symbols represent the experimental data and solid curves are the quadratic fits.

## 5 PLATFORM FOR NONLINEAR SILICON PHOTONICS

A lot of research has been conducted to investigate nonlinear effects in nano-waveguides such as stimulated Raman scattering (SRS), TPA, four-wave mixing (FWM), coherent anti-Stokes Raman scattering (CARS) [17]–[19]. Benefiting from the confined high power density of light in nano-waveguides with respect to the conventional SMF, and also taking advantage of large nonlinear Kerr coefficient of silicon, enhanced nonlinear effect is usually observed. Here, we shall demonstrate that the above presented E/O waveguide structure can be successfully deployed for high-intensity experiments and provide evidence for nonlinear behavior.

Apart from the linear scattering, the nonlinear loss resulting from TPA and TPA-induced FCA becomes dominant when higher optical power density is confined in the nano-waveguide. In our structures, a reverse biased PIN junction is used to sweep out free carriers from the waveguide region in order to reduce loss due to free carriers. Figures 6(a) and 6(b) show the experimental results from the deep-etched E/O waveguide. The in-coupled pump power (CW) was determined at 1550 nm. When the power of pump light is fixed, the output power through the waveguide rises as the applied reverse bias increases up to a certain saturation level. The reason for this is that the density of free carriers generated from TPA is proportional to the effective lifetime of free carriers, which depends upon the width of the rib waveguide and the applied reverse bias voltage [20, 21]. Before the applied bias reaches the electric field corresponding to drift velocity saturation, the effective carrier lifetime is inverse proportional to the electric field, which in turn leads to a decrease of absorption due to free carriers. In nonlinear experiments, the major concern is free-carrier induced loss because of the high generation rate of free carriers by TPA. We analyzed the impact of such free-carrier induced waveguide loss in Figure 6(a).One can find in Figure 6(a), below the saturation bias of around -20 V that the nonlinear loss is reduced effectively with increasing bias, whereas above the saturation bias voltage, free carrier associated loss then is negligible and the propagation loss is dominated by the linear scattering loss at the sidewalls. Looking at the received power at -30 V bias, we see a difference in power level between the minimum and the maximum curve of approximately 17 dB. This corresponds well to the difference in power of the in-coupled light of 12 dBm (min) and 30 dBm (max). Therefore, we conclude that the effect of

free-carrier induced loss becomes negligible within the studied power range.

Another measurement which shows evidence of nonlinear behaviour is the quadratic dependence of the photocurrent on the in-coupled pump power, as it is shown in Figure 6(b) [22]. If the nonlinear process TPA is dominant, the photocurrent was found to be proportional to the square of the confined light intensity, as explained by T.K. Liang et al. [17]. The achievement of the reduction in the FCA and quadratic relation detected proves that the here presented E/O nano-waveguide structure can be successfully deployed in nonlinear CW experiments without the limitations of previously shown structures. The integration process was appropriately optimized.

## 6 CONCLUSION

In conclusion, we have demonstrated the fabrication of low-loss SOI E/O nano-waveguides including BEOL processes. Waveguide fabrication was done in a BiCMOS technology pilot line. As a reference, nano-strip waveguides were fabricated and the analyzed experimental results are comparable with state-of-the-art. A reliable fabrication process for nano-strip waveguide with propagation loss of below 2 dB/cm is demonstrated. We have also presented the performance of the integrated E/O waveguides that exhibit the expected properties such as low linear loss for the shallow etched waveguides and integration of the E/O process without compromising waveguide performance. First nonlinear experiments could be conducted, proving the potential of the here presented technology platform for nonlinear application of silicon nano-waveguides.

## 7 ACKNOWLEDGEMENTS

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