

Design of a high efficiency CdS/CdTe solar cell with optimized step doping, film thickness, and carrier lifetime of the absorption layer

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A high-efficiency CdS/CdTe solar cell with step doped absorber layer, optimized back surface field layer, and long carrier lifetime in the absorption layer was designed. At first, The CdS/CdTe reference cell is simulated and compared with previous experimental data. In order to obtain the highest efficiency, the thickness and step doping of the absorber and back surface field layer were optimized. In addition, the effect of carrier lifetime variation in the CdTe layer on the conversion efficiency of CdTe cell was investigated. Compared with reference cell, Efficiency enhancement of the proposed structure was 4.44%. Under global AM 1.5 conditions, the optimized cell structure had an open-circuit voltage of 0.987 V, a short-circuit current density of 27.9 mA/cm² and a fill factor of 82.4%, corresponding to a total area conversion efficiency of 22.76%.

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1 INTRODUCTION

Third generation thin-film solar cells are the most promising field of photovoltaic solar cell research. They are much cheaper to manufacture (due to using simpler deposition processes), and require much less materials, as compared to the conventional single-crystal cells. Polycrystalline CdTe films have high optical absorption coefficient and are normally used in a CdS/CdTe heterojunction configuration. The most important parameter that affects photon absorption is thickness of the CdTe layer [1]. A ZnTe layer is usually used as a back surface barrier to repel the electrons at the CdTe/ZnTe heterojunction and thus decrease the loss of carriers at the back contact (due to presence of a higher band-gap layer at the back) [2]. This layer also reduces carrier recombination at the back contact due to the barrier (i.e. conduction band discontinuity) for electrons at the interface between CdTe and ZnTe layers. The electrons will reflect at this interface and will be collected with a higher probability at the CdS/CdTe heterojunction. Highly n-type CdS films are used as a suitable window layer for these cells. The thickness of CdS affects the cell's conversion efficiency. Up to a certain point, thinner CdS films produce higher short-circuit current densities [3].

The record cell efficiency of CdTe solar cells were increased by only 1.5% during the last 17 years [4]–[8]. Previous groups reported a maximum cell efficiency of 16.5% [9]–[12], but recently, First Solar research group reported a cell efficiency of 20.4% (verified by NREL) and a module efficiency of 13.9% was obtained under the lab conditions [13].

Fabrication of high-efficiency CdS/CdTe solar cells with

ultra-thin (i.e. below 1 μm) absorber layers is a challenging yet highly desirable step in improving the cell performance. Thicker absorber layers are generally used to avoid pinholes reaching through to the window layer, which may lead to shorting to the back contact. Typically, the cell performance decreases due to shunting, incomplete absorption (deep penetration loss), fully depleted CdTe layer, or interference between the main and the back contact junctions when the CdTe layer thickness approaches a certain limit. Recently N. R. Paudel et al. [14] concluded that with comprehensive cleaning of the substrates, very thin absorber layers (with only 0.25 μm of CdTe) without pinhole shorting could be deposited.

Simulation of CdTe thin film solar cells is an important strategy to test the viability of proposed structures and to predict the effect of physical changes on the cell performance. Nowadays, the challenge facing researchers and technologists is how to increase the efficiency of CdS/CdTe solar cells and therefore, decrease the gap between actual efficiency and the theoretical limit.

This paper first investigates an already-fabricated and simulated CdTe/CdS cell structure as a reference cell [2], and compares all of the simulation results with this reference cell. The improvement of the efficiency of new structures with different thicknesses of CdTe and ZnTe layers were investigated and compared to the reference cell. The effect of stepped doping grading of the BSF layer on the characteristics of the CdTe/CdS solar cells was also studied. By analyzing electrical

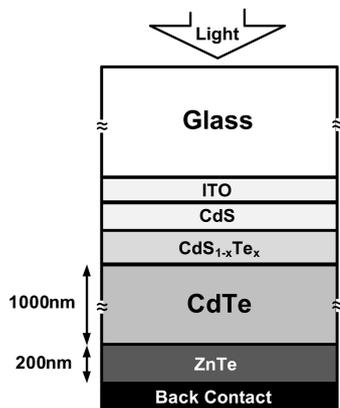


FIG. 1 Schematic structure of the reference cell [2].

characteristics of the new structure, optimum doping for the BSF layer (for achieving the highest efficiency) was obtained. Furthermore, in order to further increase the open-circuit voltage, the effect of carrier lifetime was studied. All of the simulations were done using Silvaco software [15]. These improvements resulted in a considerable improvement in the cell efficiency, as compared to the reference sample.

2 COMPARISON WITH PREVIOUS DATA

The main objective in this work was to obtain high efficiency with a reduced CdTe absorber layer thickness and to replace ZnTe layer by two layers (with different doping concentrations) in the reference CdS/CdTe cell [2]. The reference cell structure which is named structure (a) is schematically shown in Figure 1.

In the reference cell, the layers were composed of 50 nm CdS, 200 nm CdS_{1-x}Te_x (as mixed CdS/CdTe layer), 1 μm CdTe, and 200 nm ZnTe.

But there was no ITO coated glass in the reference cell. Therefore, we considered an ITO layer as transparent conducting oxide in the reference cell structure. Subsequently, this cell was modeled and its simulated characteristics were obtained.

Under AM 1.5 conditions, considering the ITO coated glass, this cell had open-circuit voltage of 925 mV, short-circuit current density of 24.82 mA/cm², fill factor of 0.798, and conversion efficiency of 18.32%. The ITO coated glass added in all simulations. Some of the most important parameters used in the simulations are shown in Table 1 [1, 2].

3 INVESTIGATION OF THICKNESS OF ZNTE LAYER ON THE CDTE CELL PERFORMANCE

Improvement of cell efficiency for different thicknesses of CdTe and ZnTe layers (corresponding to a total thickness of the CdTe and ZnTe thickness in the reference cell) was investigated. Figure 2 shows the efficiency of the cell as a function of ZnTe thickness layer.

As Figure 2 shows, at first, the device efficiency increases with increasing ZnTe thickness. This is due to enhanced absorption in the long wavelengths region. Then, after reaching a peak at about 0.8 μm the efficiency decreases, due to lower absorption in the ultra-thin CdTe layer. With these optimized thicknesses (0.8 μm ZnTe and 0.4 μm CdTe), the proposed cell showed an improved efficiency of 19.81%. The resulted structure with the optimized ZnTe thickness, which is named structure (b), is shown in Figure 3.

For comparison, characteristics of the reference cell and the structure with optimized absorber layers are shown in Figure 4. Accordingly, increasing the ZnTe thickness should improve the performance (by achieving a high J_{SC}) and at the same time, increasing V_{OC} (due to increasing absorption in the long wavelength region).

4 INVESTIGATION OF DOPANT PROFILING AND THICKNESS OF ZNTE LAYER ON CELL PERFORMANCE

In the next stage, a built-in electrical field was formed in the ZnTe layer by step-doping grading, which resulted in an in-

	CdS	CdTe	ZnTe
m_n^*/m_0	0.171	0.25	0.13
m_p^*/m_0	0.7	0.7	0.6
Dielectric Constant ϵ/ϵ_0	9.35	10.3	9.67
Electron Affinity [eV]	4.3	4.28	3.5
Electron Mobility μ_e [cm ² /Vs]	10	100	330
Hole Mobility μ_h [cm ² /Vs]	10	60	80
Electron/Hole Density n, p [cm ⁻³]	n: 10 ¹⁸	p: 10 ¹⁵	p: 10 ¹⁸
Band Gap Energy E _g [eV]	2.42	1.5	2.26
Conduction band effective density of states N _C [cm ⁻³]	2.4×10 ¹⁸	8×10 ¹⁷	7×10 ¹⁶
Valence band effective density of states N _V [cm ⁻³]	1.8×10 ¹⁹	1.8×10 ¹⁹	2×10 ¹⁹
Capture Cross Section σ_e, σ_h [cm ²]	e:10 ⁻¹⁷ h:10 ⁻¹²	e:10 ⁻¹¹ h:10 ⁻¹⁴	e:10 ⁻¹¹ h:10 ⁻¹⁶
Acceptor / Donor defect Concentration N _{DG} , N _{AG} [cm ⁻³]	A: 10 ¹⁷	D: 2×10 ¹⁴	D: 10 ¹⁶
Defect peak energy E _A , E _D [eV]	midgap	midgap	midgap
W _G [eV]	0.1	0.1	0.1

TABLE 1 Best Physical Parameters [1, 2].

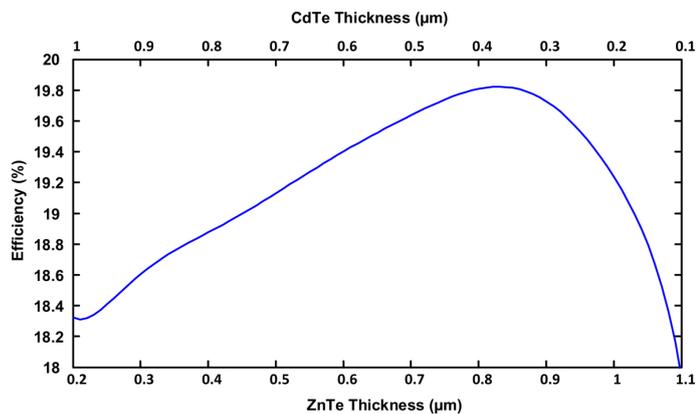


FIG. 2 Variation of cell efficiency as a function of thickness of ZnTe layer.

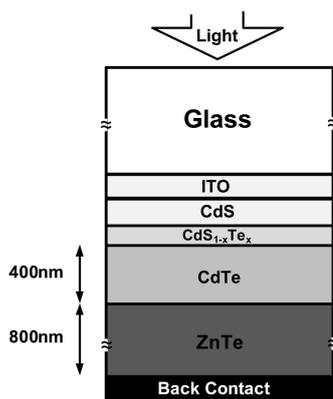


FIG. 3 Structure (a) with optimized absorption layer.

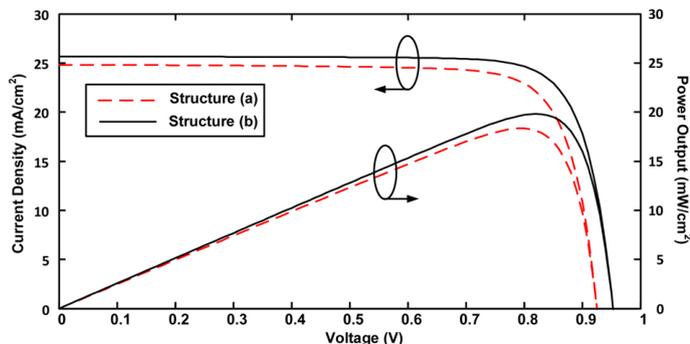


FIG. 4 Comparison of characteristics of the reference cell and the structure.

crease in the efficiency of the CdS/CdTe/ZnTe cell. This field assists carrier migration and therefore, reduces the series resistance of the cell, as well as the charge storage time. To achieve this, the ZnTe layer was divided into two layers with different doping levels. These layers were 0.6 μm thick with 10^{14} – 10^{18} cm⁻³ doping concentration (top layer) and 0.2 μm thick (reference cell default) with 10^{18} cm⁻³ doping concentration (bottom layer). This structure, which is named structure (c), is shown in Figure 5.

In this structure, doping of top ZnTe layer was varied from 10^{14} cm⁻³ to 10^{18} cm⁻³. Figure 6 shows the variation of the doping concentration of the top ZnTe layer when the doping of the ZnTe bottom layer was fixed. The efficiency was first increased with doping concentration of top ZnTe layer and then decreased after reaching 10^{16} cm⁻³ concentration. The efficiency was highest for 10^{16} cm⁻³ doping concentration due

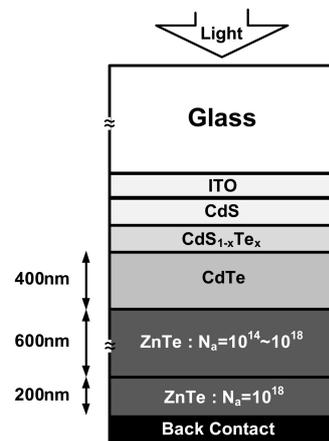


FIG. 5 Stepped doping grading of the BSF layer.

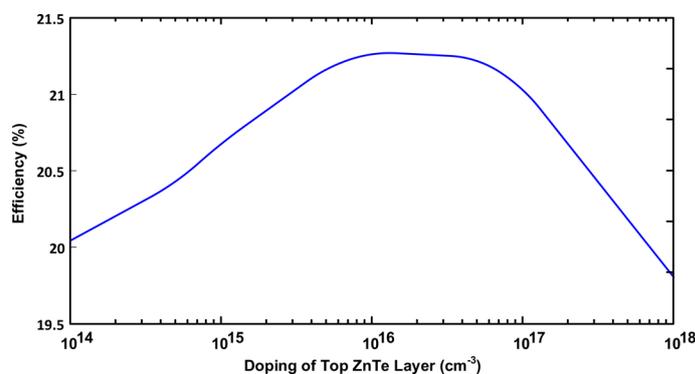


FIG. 6 Variations of efficiency as a function of the top ZnTe layer doping concentration.

to both high built-in electrical field and high absorption level. Before this optimum level, built-in electrical field is high but absorption is low and after that, built-in electrical field is low but absorption is high.

Figure 7 shows the J-V characteristics and power curve of the reference cell and the stepped doping structure. It shows a clear improvement in V_{OC} and J_{SC} of the cell with step doping design.

In the next set of simulations for more advanced results, step doping strategy was also applied to the top ZnTe layer. For this purpose, top ZnTe layer (0.6 μm thick) was divided into two layers with the same thickness, and efficiency of the cell was evaluated by variation of their doping concentrations (from 10^{14} cm⁻³ to 10^{18} cm⁻³). Figure 8 shows the proposed structure, which is named structure (d), for this set of simulations.

The variation of the cell efficiency for different doping of top ZnTe layers (i.e. two 300 nm thick layers) is shown in Figure 9. As it can be seen from this Figure, the efficiency does not increase by the step doping of the top ZnTe layer and it is maximum for 10^{16} cm⁻³ doping concentration of the two 300 nm thick ZnTe layers. Therefore, the cell efficiency does not increase by dividing the 600 nm thick ZnTe layer into two 300 nm thick layers.

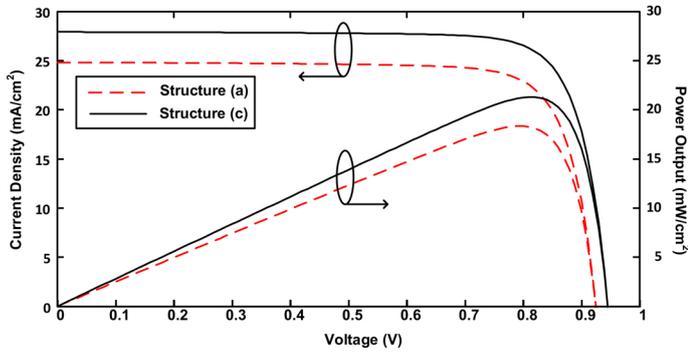


FIG. 7 J-V and power curves of the reference cell and stepped doping structure.

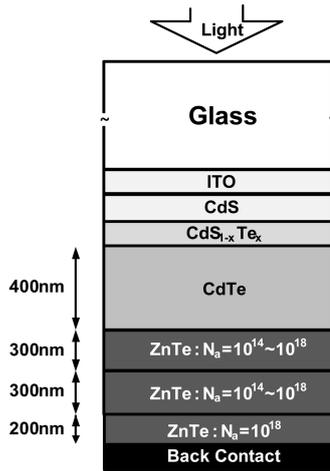


FIG. 8 Step doping grading of the top ZnTe layer (Film thicknesses are not plotted with respective scales).

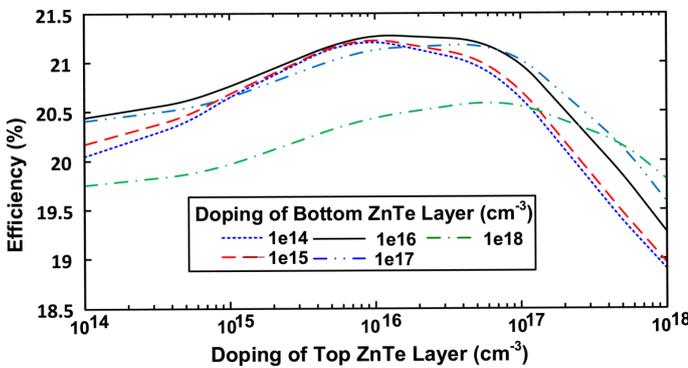


FIG. 9 Efficiency of the cell for step doping grading in the Top ZnTe layer.

5 CARRIER LIFETIME IN CDTE LAYER

The carrier lifetime of CdTe, which is the key parameter for the voltage calculations, also has a strong influence on the solar cell fill-factor. In order to improve the efficiency further, the basic parameters (J_{SC} , V_{OC} , FF and Efficiency) of the proposed cell were obtained as a function of carrier lifetime in the CdTe layer. The results are shown in Figure 10. The variations of carrier lifetime in the model were obtained with variation of defect density.

Increased defect density and purity of the CdTe alters the electron lifetime as well as the hole lifetime. Physically, a reduction in the defect density could be the key to improvement in

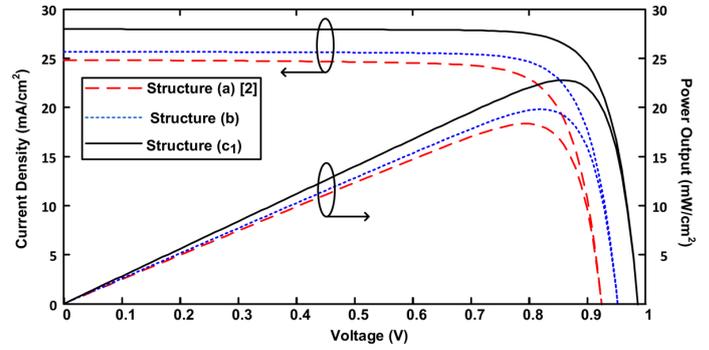


FIG. 11 Current density-voltage and power output of the CdS/CdTe solar cell for three structures at 1 sun AM1.5 illumination. Structure (a) is reference cell. Structure (b) is step doped structure and structure (c₁) is structure (c) with optimized step-doping grading and thickness of BSF layer and long carrier lifetime in CdTe layer.

increased lifetime through a smaller number of recombination centers.

Therefore, at higher lifetimes, essentially all carriers generated in the depletion region will be collected. Consequently, the V_{OC} and hence, the conversion efficiency, should improve with increasing the carrier lifetime. An equation for V_{OC} is found by:

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right) \quad (1)$$

Where n is the ideally factor, k Boltzmann's constant, T absolute temperature, J_0 dark current density, J_{SC} short current density and q electrical charge. J_0 is directly linked to the defect density and purity of the material (a higher lifetime corresponds to a purer or low defect density material). With this formula, if J_{SC} saturates, V_{OC} can be increased if J_0 decreases. Obviously, as simulations predicted, longer carrier lifetimes resulted in a higher V_{OC} . As a result, the conversion efficiency increases with increasing carrier lifetime.

Our simulation results indicated that if the carrier lifetime is equal to 10 ns [16], the efficiency can be as high as 22.76%.

Figure 11 shows J-V and power characteristics comparison between three structures under AM1.5 illumination at 1 sun. (a) is the reference cell, (b) is the step-doped cell, and (c₁) is the structure (c) with optimized step doping structure and optimized thickness of BSF layer, and long carrier lifetime in CdTe layer. As this Figure shows, the short current density for proposed structure (c₁) is as high as 27.9 mA/cm² corresponding to an efficiency of 22.76% due to step doping grading and long carrier lifetime in CdTe layer. For comparison, the open-circuit voltage, short-circuit current, fill factor and conversion efficiency for different structures are given in Table 2.

6 CONCLUSION

Several step-doped profiles in the BSF layer of CdS/CdTe cells were evaluated. Optimization of the location of homo-junction and doping concentrations during the step doping grading resulted in a conversion efficiency of 21.28%. This result showed a noticeable improvement over the 18.32% efficiency of the reference sample which had a uniform doping

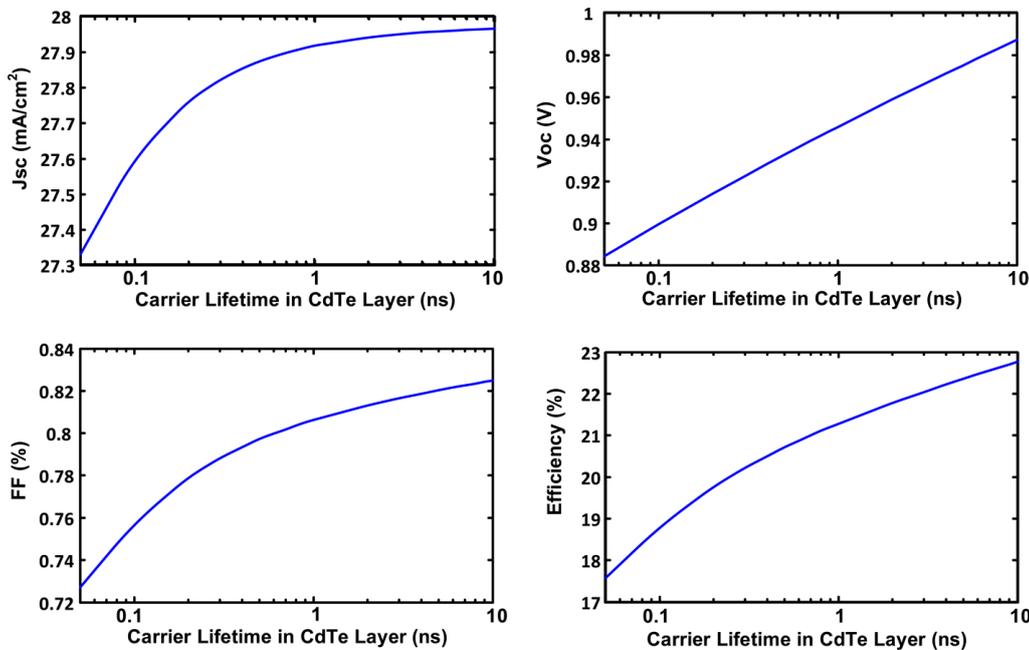


FIG. 10 Basic parameters of the cell as a function of the CdTe layer’s carrier lifetime.

profile in the absorber layer. Subsequently, the effect of carrier lifetime in the CdTe layer on the performance of CdS/CdTe cell was investigated. The maximum conversion efficiency of 22.76% ($V_{OC} = 0.987$ V, $J_{SC} = 27.9$ mA/cm², FF = 0.824) was achieved with the proposed cell consisting of 0.2 μm ZnTe bottom layer with 10¹⁸ cm⁻³ doping concentration, 0.6 μm ZnTe top layer with 10¹⁶ cm⁻³ doping concentration, 0.4 μm CdTe layer with 10 ns carrier lifetime, and 50 nm CdS layer thickness. Practically, these modifications should not be difficult to be implemented during the fabrication process.

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	J_{SC} (mA/cm ²)	V_{OC} (v)	FF (%)	Efficiency (%)
Structure (a) [Simulated]	24.82	0.925	0.798	18.32
Structure (b)	25.66	0.952	0.81	19.81
Structure (c)	27.91	0.945	0.806	21.28
Structure (c ₁)	27.9	0.987	0.824	22.76
Structure (c ₁) (Structure (c) by optimized step doping grading and thickness of BSF layer and long carrier lifetime in CdTe layer)				

TABLE 2 Output Parameters of Different Cells.

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